

# Design of Half-Bridge Piezo-Transformer Converters in the AC Adapter Applications

Sungjin Choi, Taecil Kim and Bo. H. Cho  
School of Electrical Engineering, Seoul National University  
San 56-1, Shillim-dong Gwanak-gu  
Seoul, 151-742, Korea  
zerotics@yahoo.co.kr

**Abstract**—As a viable alternative to magnetic transformers in the power supply for portable electronics, this paper presents a miniaturized off-line travel adapter or charger for cellular phones using the piezoelectric transformer. Various design considerations in the design of ac PT adapters are investigated before coming up with the proposed pseudo-resonant topology. A prototype hardware design is also presented and verified by simulations and experiments..

## I. INTRODUCTION

As the piezoelectric transformer (PT) technology develops, PTs may become a viable alternative to magnetic transformers in various applications. Power supplies that employ PTs, rather than the classical magnetic transformers [1,2], could be made smaller in size. This paper presents a miniaturized off-line travel battery charger for cellular phones using the piezoelectric transformer as a main energy transferring component in the ac-dc adapter [9].

The schematic diagram of a piezoelectric transformer adapter is presented in Fig. 1. An inverter is used to drive the PT whose driving frequency is determined by the PT's mechanical resonant frequency and the gain characteristic of the PT.

Since the PT acts as a band-pass filter, only the fundamental frequency passes through the PT. The topology used to drive the PT has to provide a low-harmonic-content ac waveform, which is tuned to be near the PT mechanical resonant frequency ( $f_m$ ) in order to minimize the circulating energy through the inherent input capacitance of the PTs. In addition, the off-line application has a high voltage (~400V) DC link and should provide a scheme to reduce the capacitive turn-on losses due to the parasitic capacitance of the small packaged high-voltage switch component (400V MOSFET in DPAK).

It was shown in [4,5] that by using specific characteristics of the PT with a half-bridge topology, ZVS could be achieved without any additional elements. This scheme may be useful when the load impedance is nearly fixed, as in the

lamp ballast case. However, it utilizes a very narrow inductive region, which is highly dependent on the load impedance variations, and thus, this scheme cannot be applied to wide load range applications such as AC adapters.

Therefore, some PT primary circuits adopt additional series inductors to achieve the ZVS condition and the waveform shaping ( $L_s$ -type) [11]. The resonance formed by the series inductor and the internal input capacitance of the PT. However, a bulky series inductor has to be designed to provide both the primary side current and the ZVS current. Thus, the PT advantages of small size were inadvertently lost. Some papers [8] have utilized half-bridge pseudo-resonant branches to provide the soft-switching characteristics. This scheme has been derived from the topological classification that has been referred to as the zero-voltage-switching clamped-voltage (ZVS-CV), partial-resonant, quasi-square wave, or the resonant transition topologies [7].

In this paper, the pseudo-resonant ( $C_s$ - $L_p$  type) half-bridge converter is adopted. In this circuit, the capacitance,  $C_s$ , together with the parallel inductance,  $L_p$ , are considered to be the parameters to be optimally designed so as to provide a nearly sinusoidal waveform to the PT. By this design process, reduced switching losses and efficient PT energy conversion are obtained simultaneously in offline applications.

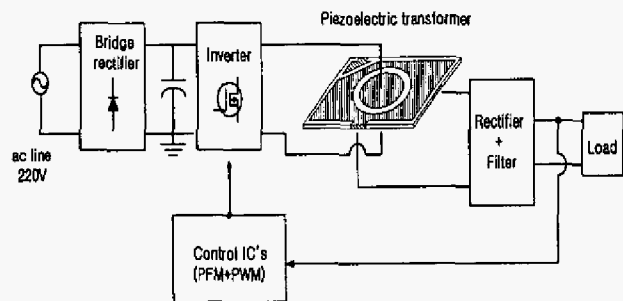


Fig.1 A general arrangement of PT adapters

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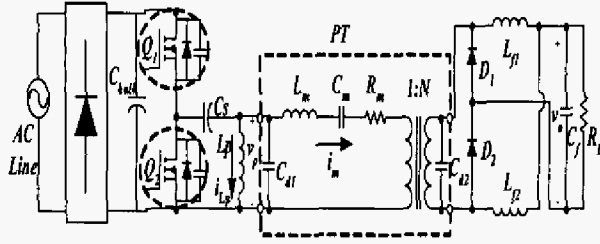


Fig.2 The pseudo-resonant (Cs-Lp type) half bridge ac adapter using PT

## II. PRINCIPLE OF OPERATION AND DESIGN OF THE HALF-BRIDGE PT ADAPTER

### A. Analysis of the pseudo-resonant half-bridge inverter

A pseudo-resonant half-bridge PT driver is shown in Fig.2. The PT is represented by an equivalent series-parallel resonant circuit. The parameters  $L_m$ ,  $C_m$ ,  $R_m$  represent the mechanical behavior of the PT, and  $C_{d1}$  and  $C_{d2}$  are the capacitances of the primary and secondary electrodes, respectively[9]. A resonant inductor ( $L_p$ ) is placed in parallel with the PT and a resonant capacitance ( $C_s$ ) is placed between the switch leg and the PT.

The mode of operations and their corresponding waveforms are illustrated in Fig.3. The gate drive waveform contains a sufficient deadtime for the ZVS condition. In this section, detailed analysis and the derivation of the design equation is performed.

#### 1) During the switch ON/OFF : Resonant PT input waveforms

During the MOSFET switch on or off stage, the series capacitance,  $C_s$ , resonates with the parallel inductance,  $L_p$ , which provides a nearly sinusoidal voltage to the PT primary side. Because the PT has a very high resonant quality factor, input current  $i_m(t)$  can be assumed to be pure sinusoidal and equal to  $I_m$  at time  $t=0$ , then

$$i_m(t) = I_m \cos(\omega t) \quad (1)$$

where,  $\omega$  is the switching frequency of the circuit.

When the high-side switch is turned on at  $t=t_1$ , the primary voltage of the PT and the parallel inductor current are given by

$$\begin{aligned} v_p(t) &= K\omega \cdot \sin[\omega(t-t_1)] + V_{po} \cdot \cos[\omega_o(t-t_1)] \\ &\quad - [Z_o(I_{Lpo} + I_m) + K\omega] \cdot \sin[\omega_o(t-t_1)] \\ i_{Lp}(t) &= -K \cdot \cos[\omega(t-t_1)] + (I_{Lpo} - K) \cos[\omega_o(t-t_1)] \quad (2) \\ &\quad + \frac{V_{po}}{Z_o} \sin[\omega_o(t-t_1)] \end{aligned}$$

$$A = \frac{I_m}{1 - \left(\frac{\omega_o}{\omega}\right)^2}, \quad \omega_o = \frac{1}{\sqrt{L_p(C_s + C_{d1})}}, \quad Z_o = \sqrt{\frac{L_p}{C_s + C_{d1}}}$$

where,  $V_{po}$  and  $I_{Lpo}$  are initial values of the resonant period.

When the low-side switch is turned on, the waveforms are similar to (2). Equation (2) generates a piecewise sinusoidal voltage waveform which is applied to the PT.

Therefore a low-harmonic-content waveform is used to drive the PT.

#### 2) During the Dead-time : Derivation of the ZVS condition

To achieve a ZVS condition in the MOSFETs, their parasitic capacitances should be fully charged or discharged during the gate dead-time,  $T_d$ . This condition is achieved by using a parallel inductor,  $L_p$ . Thus the voltage waveform of the drain to source terminal is a quasi-square waveform.

Assuming that the current in the parallel inductor,  $i_{Lp}$ , is constant during the short transition time, there should be a sufficient current to transit the voltage on the drain-to-source capacitor before the next gate pulse is applied. Thus, the minimum required current ( $I_{req}$ ) is given by,

$$I_{req} = C_{eq} \frac{V_{dc}}{T_d} \quad (3)$$

$$C_{eq} \approx C_{ds1} + C_{ds2} + C_{d1}$$

where  $V_{dc}$  is the voltage rectified from the ac line,  $T_d$  is the dead-time period,  $C_{d1}$  is the PT primary electrode capacitance, and  $C_{ds1}$  and  $C_{ds2}$  are the parasitic capacitances of  $Q_1$  and  $Q_2$ , respectively.

When  $C_s$  is relatively large, the resonant voltage,  $v_p(t)$ , can be approximated by the fundamental harmonic of magnitude of  $V_{pm}$  given by

$$V_{pm} \approx V_{dc} \cdot \left(\frac{2}{\pi}\right) \cdot \frac{\sin\left(\pi \frac{T_d}{T}\right)}{\pi \frac{T_d}{T}} \quad (4)$$

Here it is assumed that the switching frequency of the converter is near the resonant frequency of the PT, the PT

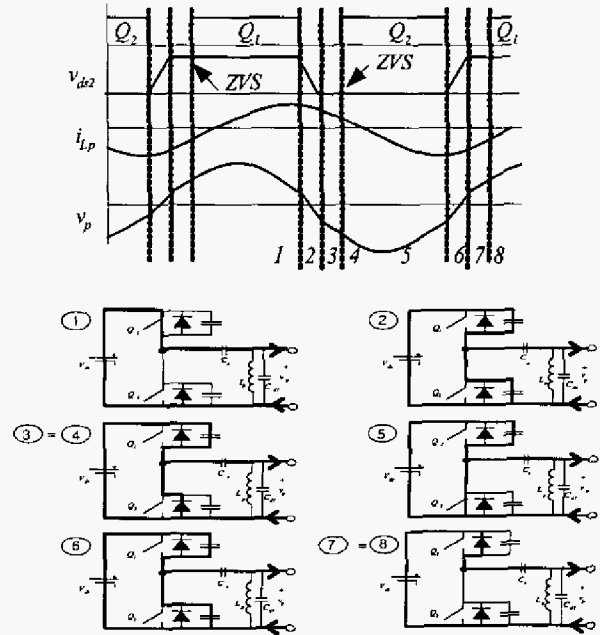


Fig.3 Waveforms and operation modes of the PT driving circuit

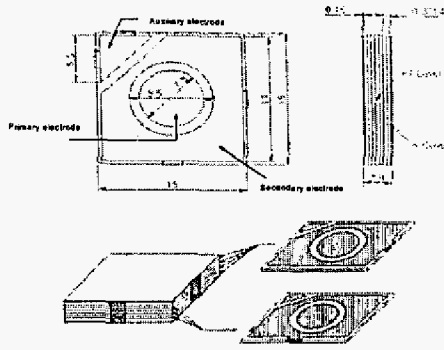


Fig.4 Physical layout of the PT sample used in this paper

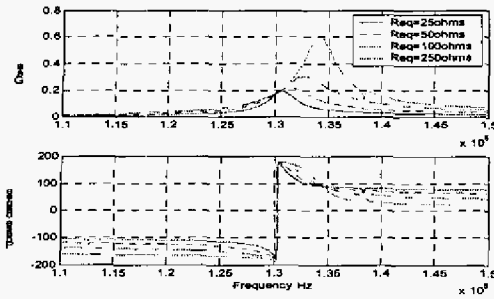


Fig.5 PT gain curves vs. frequency with variable load resistance

input current will cross zero during the dead-time. Therefore, the inductor current in the beginning of the dead-time region determines the ZVS operation, and can be approximated by

$$I_{Lp_o} = \frac{V_{pm}}{2\pi \cdot f \cdot L} \cdot \cos\left(\pi \frac{T_d}{T}\right) \quad (5)$$

$$= \left(\frac{2}{\pi}\right) \cdot \frac{\sin\left(2\pi \frac{T_d}{T}\right)}{2\pi \frac{T_d}{T}} \cdot \frac{V_{dc}}{2\pi \cdot f \cdot L}$$

where  $T=1/f$  is the switching period.

From (3) and (5), an inductance value for the ZVS is derived. The maximum  $L_p$  should be designed to be

$$L_p \leq \left(\frac{2}{\pi}\right) \cdot \frac{\sin\left(2\pi \frac{T_d}{T}\right)}{2\pi \frac{T_d}{T}} \cdot \frac{T_d \cdot T}{2\pi \cdot C_{eq}} \quad (6)$$

### B. Analysis of current-doubler output rectifier stage

The generated charges on the output electrode caused by a mechanical vibration of the PT performs as a sinusoidal voltage source. Among various voltage-driven-type rectifier topologies, a current-doubler is adopted because only half of the output current is processed in each output inductor. Thus the effective ripple current on the output filter capacitor is reduced, which will reduce the output filter size. Output filter

inductors,  $L_{p1}$  and  $L_{p2}$ , are charged alternately providing nearly half of the output current and can be implemented with low-profile surface mount (SMD) type inductors.

To calculate the voltage conversion ratio of the PT, the input impedance of the output rectifier stage must be derived. This can be assumed to be a pure resistor,  $R_{eq}$ , because the input voltage and current waveforms have the same phase[3]. By using a first-order harmonic approximation and some calculations,  $R_{eq}$  is obtained as

$$R_{eq} = \frac{\pi^2}{2} \left(1 + \frac{V_F}{V_o}\right)^2 R_L \quad (7)$$

where,  $V_F$  is the output diode forward voltage drop,  $V_o$  is the output dc voltage, and  $R_L$  is the load resistance.

### C. Piezoelectric transformer

Figure 4 shows the structure of the 5W multi-layered PT sample used in this paper. The primary and the secondary electrode are placed on the inner and outer section of the PT, respectively. Its mechanical resonant frequency is about 130kHz. The measured parameter values for the equivalent circuit in Fig.2 are as follows:  $C_{q1}=331$ [pF],  $R_m=34.6$ [ $\Omega$ ],  $L_m=40.9$ [mH],  $C_m=37.0$  [pF],  $N=0.23$ ,  $C_{d2}=13.5$ [nF].

From (7), the equivalent resistance of the output rectified stage is obtained and is used for the gain calculation of the PT. The PT gain curve is derived as in Fig.5, with a variable load resistance of the PT. From the gain curve, the minimum driving frequency of the adapter circuit is determined.

## III. HARDWARE IMPLEMENTATION AND PERFORMANCE ANALYSIS

A prototype 5W adapter / Li-ion battery charger for the cellular phones is designed and constructed as in Fig. 6. The specifications of the target system are :

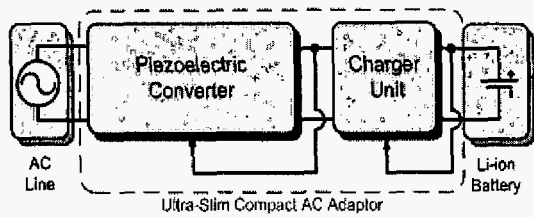
- AC input voltage :  $220 \pm 10\%$  [V<sub>rms</sub>]
- Line frequency : 60 Hz
- Regulated output voltage : 5 V
- Maximum output current : 1 A

Power stage components are :

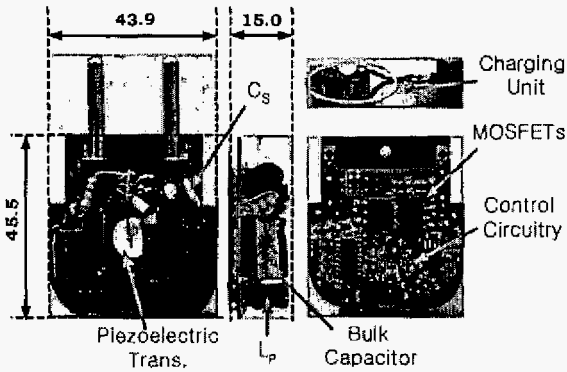
- Bridge rectifier : MB4S (GE)
- Bulk capacitor : 400V 4.7uF Electrolytic. (Rubicon)
- MOSFET : FQD2N40/FQD2P40 (400V/1A DPAK Coss:40pF@400V, Fairchild)
- Resonant tank :  
Cs=3.2nF(1kV ceramic), Lp=2.7mH(Axial  $\phi$ 7)
- Piezo Transformer : PZT #4A-1 (Dong-il Tech.)
- Output inductor : 100uH/0.5A SMD (TDK)
- Output capacitor : 220uF/10V SMD Tantal (Hitachi)

Control stage consists of:

- Controller : TL494 with external VCO circuit
- Frequency control range : 131kHz<f<140kHz (above resonant frequency)
- Opto-isolator : PC817
- Output regulator : TL431

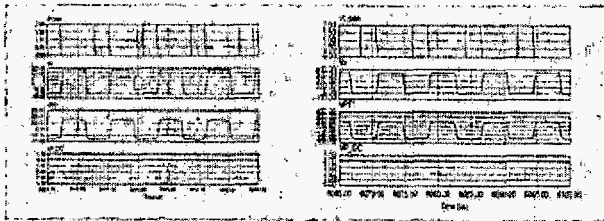


(a) Circuit Configuration



(b) Photograph of the 5W prototype hardware [unit : mm]

Fig. 6. Low-profile AC Adapter/Charger using the PT

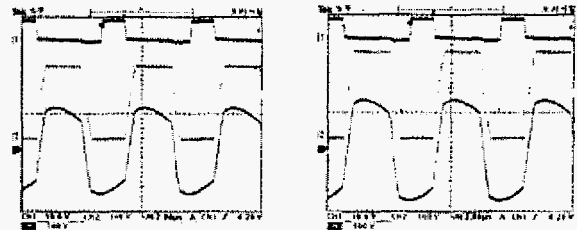


(a)  $V_{ac}=198$  [V<sub>rms</sub>] (b)  $V_{ac}=242$  [V<sub>rms</sub>]

Fig.7 Simulation waveforms

(ch1: low side gate, ch2: drain-to-source voltage  
ch3: PT primary voltage, ch4: output voltage )

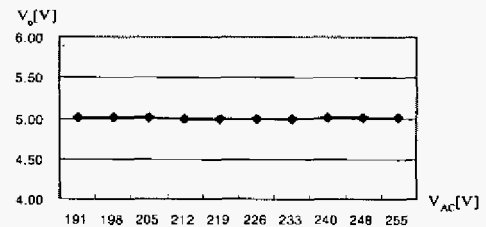
Figure 7 and 8 show the PT driving circuit waveforms in the two extreme input conditions. As predicted from the analysis, the drain-to-source voltage is a trapezoidal shape which accomplishes a ZVS operation successfully, and the PT input waveform is nearly sinusoidal. Figure 9 and 10 show the performance of the hardware system. With the proposed resonant driving method, increase of PT operating efficiency of 1~2% was obtained.



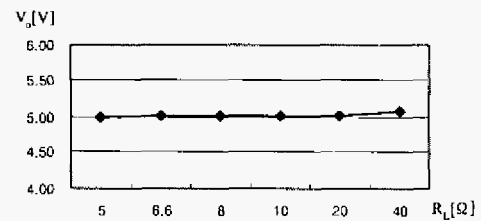
(a)  $V_{ac}=198$  [V<sub>rms</sub>]

(b)  $V_{ac}=242$  [V<sub>rms</sub>]

Fig.8 Hardware waveforms  
(ch1: low side gate, ch2: drain-to-source voltage,  
ch3: PT primary voltage )



(a) line regulation



(b) load regulation

Fig.9 Output characteristics

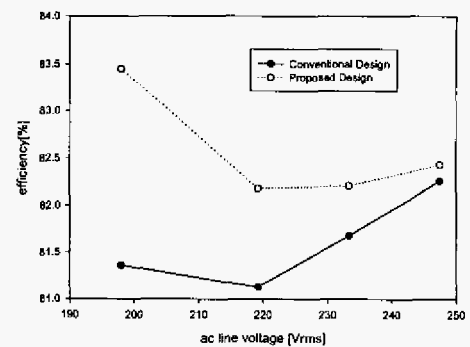


Fig.10 Efficiency of the PT vs line ( Maximum load condition)

#### IV. CONCLUSION

This paper presents a pseudo-resonant topology which is suitable for the off-line piezo-adapter. The proposed topology provides a nearly sinusoidal voltage on the primary side of the PT to reduce the circulating energy utilizing a partial resonance during the dead-time. The resonance characteristics provide additional gain of the inverter which eases the PT voltage gain design. During the gate dead-time, the parallel inductor branch also provides a ZVS condition to both of the main switch pairs. A design of the ac piezo-adapter using the above topology is also presented and verified by simulations and experiments.

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